SPECIFICATIONS AND FEATURES

DATASHEET

WWW.UNICORE.COM

# UC6580x-00

## Dual-Frequency GNSS Positioning Chip

# Foreword

## Scope

This datasheet provides information on the hardware features and performance specifications of UC6580x-00 positioning chip.

### Target Readers

This datasheet applies to technicians who have knowledge in the GNSS field but not to general readers.

## Statement

### Legal right notice

This manual provides information and details on the products of Unicore Communication, Inc. (“Unicore”) referred to herein.

All rights, title and interest to this document and the information such as data, designs, layouts contained in this manual are fully reserved, including but not limited to the copyrights, patents, trademarks and other proprietary rights as relevant governing laws may grant, and such rights may evolve and be approved, registered or granted from the whole information aforesaid or any part(s) of it or any combination of those parts.

Unicore holds the trademarks of “和芯星通”, “Unicore”, “UNICORECOMM” and other trade name, trademark, icon, logo, brand name and/or service mark of Unicore products or their product serial referred to in this manual (collectively “Unicore Trademarks”).

This manual or any part of it, shall not be deemed as, either expressly, implied, by estoppel or any other form, the granting or transferring of Unicore rights and/or interests (including but not limited to the aforementioned trademark rights), in whole or in part.

### Disclaimer

The information contained in this manual is provided “as is” and is believed to be true and correct at the time of its publication or revision. This manual does not represent, and in any case, shall not be construed as a commitments or warranty on the part of Unicore with respect to the fitness for a particular purpose/use, the accuracy, reliability and correctness of the information contained herein.

Information, such as product specifications, descriptions, features and user guide in this manual, are subject to change by Unicore at any time without prior notice, which may not be completely consistent with such information of the specific product you purchase.

Should you purchase our product and encounter any inconsistency, please contact us or our local authorized distributor for the most up-to-date version of this manual along with any addenda or corrigenda.

# Revision History

| Version | Revision History | Date |
|---|---|---|
| R1.0 | First Release. | Sep. 2023 |
| R1.1 | Updated the working voltage in technical specifications;<br>Updated the IO power domain description;<br>Updated Table Analog Electrical Specifications 1. | Oct. 2023 |
| R1.2 | Updated the model to UC6580x-00 by adding sub-model;<br>Updated the description of pin 20;<br>Updated the description related to I2C;<br>Updated the table in section Ordering Information. | Jan. 2024 |
| R1.3 | Updated the V_BACK voltage;<br>Updated the description of V_BACK. | Mar. 2024 |
| R1.4 | Updated the main power voltage and IO voltage to 1.7 V ~ 3.6 V.<br>Added thermal resistance in **1.3 Technical Specifications**.<br>Refined the description of pin4 in **2.2.2 Analog Pin**.<br>Removed the information about backup battery in **3.2 Power Management Unit**.<br>Corrected the PIO of SPI master in **5.1.3 SPI master**.<br>Added I2C timing requirements in **5.1.4 I2C**.<br>Modified section **6.2 "BOOT Mode"** to "**Firmware Upgrade Mode**" and updated the time period that the CPU detects a firmware upgrade request.<br>Added temperature conditions in **7 Electrical Specifications**.<br>Removed V_CORE in **7.1 DC Electrical Specifications** and added description of V_CORE in **3.2 Power Management Unit**.<br>Updated the min. of TCXO_IN and added the recommended inductance and capacitance for DCDC_OUT in **7.1.1 Absolute Maximum Ratings**.<br>Added section **7.2 PIO Electrical Specifications**.<br>Updated the LDO_RET, DCDC_OUT, and TCXO_IN_Vpp, added the recommended inductance and capacitance for DCDC_OUT in **7.3 Analog Electrical Specifications**.<br>Modified the typical value of L1_IN in **7.4 RF Electrical Specifications**.<br>Updated the picture of the product in **10.1 Product Appearance**.<br>Added section **10.3 Moisture Sensitivity Level**. | Mar. 2025 |

| Version | Revision History | Date |
| --- | --- | --- |
| R1.5 | Updated the min. of TCXO_IN in **7.1.1 Absolute Maximum Ratings**. | Jun. 2025 |
| R1.6 | Updated the reacquisition sensitivity and added the power consumption of LDO mode in **1.3 Technical Specifications**.<br>Added **PIO State After Power-On** in **2.2.3 PIO Pin Description**.<br>Modified the diagram (added FLASH) in **3.2 Power Management Unit**.<br>Added notes regarding the external RTC clock in **3.3 Clock**.<br>Added **7.2 Transient Maximum Ratings**.<br>Modified the pin names: pin1/4/39 modified from NC to RSV, pin15 modified from TCK to PIO18, pin16 modified from TMS to PIO17. | Oct. 2025 |
| R1.7 | Text description correction: In RTC time keeping mode, the storage location of relevant data was changed from retention RAM to flash. | Nov. 2025 |

# Product Introduction

## 1.1 Overview

UC6580x-00 is a dual-frequency multi-constellation positioning SoC developed by Unicore Communications, with sub-meter level accuracy, supporting BDS-3 signals. It adopts 22 nm process, low-power design, compact size, RF-baseband integrated technology, and supports multi-path mitigation, anti-jamming and high precision GNSS joint positioning, which performs well in the power and size sensitive scenarios.

UC6580x-00 is suitable for global applications. It has 96 tracking channels, supports GPS, GLONASS, BDS, Galileo, NavIC and QZSS multi-constellation joint positioning, as well as SBAS signal reception processing, providing fast and accurate positioning experience with high performance.

UC6580x-00 supports L1 + L5/L2 dual-frequency single point positioning and RTD, as well as AGNSS. It is suitable for wearables, handheld devices and walking navigation, significantly improving users' experience compared with single-frequency solution especially in urban multi-path environment.

UC6580x-00 has two models including automotive grade and industrial grade.

| Model | Grade | Package |
|---|---|---|
| UC6580A-00 | Automotive | QFN40 |
| UC6580I-00 | Industrial | QFN40 |

## 1.2 Product Features

- 22 nm dual-frequency multi-constellation GNSS SoC, with low power consumption and compact size
- Concurrent acquisition and tracking of dual frequencies from multiple constellations, including BDS-3 signals; supports:
    - BDS B1I/B1C* + B2a or B1I/B1C* + B2I
    - GPS L1 + L5 or L1 + L2
    - Galileo E1 + E5a or E1 + E5b
    - GLONASS G1 or G1+G2
    - QZSS L1 + L5 or L1 + L2
    - SBAS L1

- NavIC L5*

- Real-time wideband and narrowband anti-jamming technology: detection and removal of wideband and narrowband jamming of no less than -75 dBm
- Supports L1 + L5/L2 dual-frequency single point positioning and sub-meter level RTD positioning, with excellent multi-path mitigation algorithm
- RF and baseband design with ultra-high sensitivity: acquisition sensitivity better than -148 dBm, tracking sensitivity better than -162 dBm
- Supports AGNSS
- Supports secure boot
- Automotive grade and industrial grade with QFN40 package (See the section Ordering Information for more details)
- Conforms to the requirement of AEC-Q100 Grade2 (UC6580A-00)

*. Supported by specific firmware. ↩

## 1.3 Technical Specifications

| Basic Information | | | |
|---|---|---|---|
| **Channel** | 96 Channels | | |
| **Update Rate** | 10 Hz (max.) | | |
| **Data Format** | NMEA-0183，Unicore，RTCM 3.x | | |
| **Frequency** | | Mode 1 | Mode 2* |
| | BDS | B1I/B1C* + B2a | B1I/B1C* + B2I |
| | GPS | L1 + L5 | L1 + L2 |
| | Galileo | E1 + E5a | E1 + E5b |
| | GLONASS | G1 | G1 + G2 |
| | QZSS | L1 + L5 | L1 + L2 |
| | NavIC | L5* | - |
| | SBAS | L1 | L1 |

| | |
|---|---|
| **Observation Accuracy** | |
| Horizontal Accuracy (RMS) | Single point positioning: 1.5 m |
| Vertical Accuracy (RMS) | Single point positioning: 2.5 m |
| Time Accuracy (RMS) | 5 ns，peak-to-peak value 30 ns (24h) |
| Velocity Accuracy[1] | 0.02 m/s |
| **TTFF[2]** | |
| Cold Start | 26 s |
| Hot Start | 2 s |
| Reacquisition | 1 s |
| **Sensitivity[3,4]** | **GNSS** |
| Cold Start | -148 dBm |
| Hot Start | -156 dBm |
| Tracking | -162 dBm |
| Reacquisition | -160 dBm |
| **Power Consumption (@25°C)[5]** | |
| DCDC Mode | Acquisition: 40 mA @ 3 V<br>Tracking: 40 mA @ 3 V |
| LDO Mode | Acquisition: 96 mA @ 3 V<br>Tracking: 96 mA @ 3 V |
| Backup Mode | 5 μA @ 3 V |
| **Thermal Resistance (@25°C)** | |
| ThetaJA | 44.96 °C/W |
| ThetaJB | 11.48 °C/W |
| **Working Voltage** | |
| Main Power Supply | 1.7 V to 3.6 V |

| | |
|---|---|
| **IO Power Supply** | 1.7 V to 3.6 V |
| **Backup Power Supply** | 1.7 V to 3.6 V |
| **Communication Interfaces** | |
| UART x 2 | |
| I2C x 1 | |
| SPI[6] x 2 | |
| **Reliability Test and Certificates** | |
| **Reliability** | Conforms to JESD47 standard (UC6580I-00) |
| | Conforms to AEC-Q100 Grade2 standard (UC6580A-00) |
| **Certificates** | Conforms to RoHS and REACH requirements |

o. Supports RTCM3.x input ↩

*. Supported by specific firmware. ↩

1. Uniform linear motion of -33 mps using a simulator. ↩

2. Satellite signal strength @ -130 dbm. ↩

3. To get the sensitivity index, CN0 needs to achieve 41 dB (The performance might be updated). ↩

4. Connect to a matched external LNA to ensure superior performance. ↩

5. Depends on the firmware version. ↩

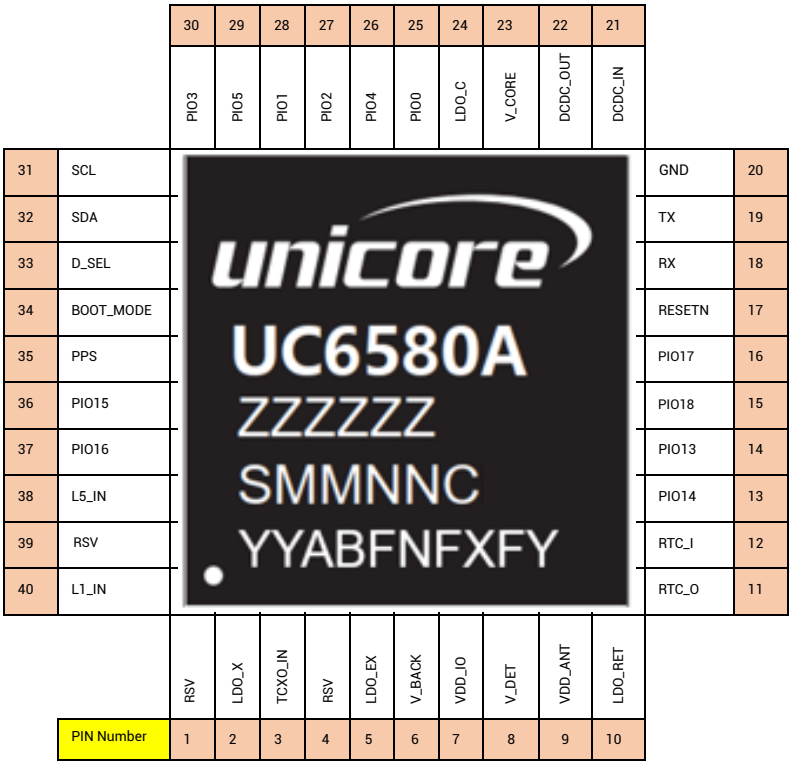
6. Not supported currently. ↩

# Pin Definition

## 2.1 Pin Assignment

UC6580A-00 and UC6580I-00 have the same pins, and the figure below gives the diagram of UC6580A-00 as an example.

QFN40 TOP VIEW (Marking Side)



## 2.2 Pin Description

### 2.2.1 Power Supply Pin

| Name | Pin | Type | Description |
|---|---|---|---|
| DCDC_IN | 21 | Power | DC/DC power input.<br>(DCDC_IN and VDD_IO are required<br>to use the same external power supply.) |
| DCDC_OUT | 22 | Power | DC/DC power output |
| V_CORE | 23 | Power | Core power input |
| V_BACK | 6 | Power | Backup power input |
| VDD_IO | 7 | Power | IO/TCXO power input.<br>(DCDC_IN and VDD_IO are required<br>to use the same external power supply.) |
| LDO_C | 24 | Power | Core LDO voltage output |
| LDO_X | 2 | Power | TCXO LDO voltage output |
| LDO_EX | 5 | Power | Used by the chip itself, and cannot<br>supply power to other circuits |
| GND | 20 | - | Connect to Ground |
| V_DET[1] | 8 | Power | Antenna detection power input |
| VDD_ANT | 9 | Power | Antenna power output |
| LDO_RET | 10 | Power | Backup power output |
| GND | | | Ground |

[1]. Not supported currently.

## 2.2.2 Analog Pin

| Name | Pin | Type | Description |
|---|---|---|---|
| L1_IN | 40 | RF | L1 RF input |
| L5_IN | 38 | RF | L5 or L2 RF input |
| TCXO_IN | 3 | Clock | 26 MHz TCXO input |
| RTC_I | 12 | Clock | 32.768 kHz crystal or digital waveform input |
| RTC_O | 11 | Clock | 32.768 kHz clock output |
| RSV | 4 | - | Leave floating or connect to GND.<br>Recommended to connect to GND. |
| RSV | 39 | - | Reserved, leave floating. |
| RSV | 1 | - | Reserved, leave floating. |

## 2.2.3 PIO Pin Description

| Name | Pin | Type | IO Reset | Description |
|---|---|---|---|---|
| PIO0 | 25 | IO | I/Pull-up | GPIO0 |
| PIO1 | 28 | IO | I/Pull-up | GPIO1 |
| PIO2 | 27 | IO | I/Pull-up | GPIO2 |
| PIO3 | 30 | IO | I/Pull-up | GPIO3 |
| PIO4 | 26 | IO | I/Pull-up | GPIO4 |
| PIO5 | 29 | IO | I/Pull-up | GPIO5 |
| TX | 19 | IO | I/Pull-up | GPIO6 |
| RX | 18 | IO | I/Pull-up | GPIO7 |
| SCL | 31 | IO | I/Pull-up | GPIO8 |
| SDA | 32 | IO | I/Pull-up | GPIO9 |
| D_SEL | 33 | IO | I/Pull-up | GPIO10 |
| PPS | 35 | IO | I/Pull-up | GPIO11 |

| Name | Pin | Type | IO Reset | Description |
| --- | --- | --- | --- | --- |
| BOOT_MODE | 34 | IO | I/Pull-up | GPIO12 |
| PIO13 | 14 | IO | I/Pull-up | GPIO13 |
| PIO14 | 13 | IO | I/Pull-up | GPIO14 |
| PIO15 | 36 | IO | I/Pull-up | GPIO15 |
| PIO16 | 37 | IO | I/Pull-up | GPIO16 |
| PIO17 | 16 | IO | I/Pull-up | GPIO17 |
| PIO18 | 15 | IO | I/Pull-up | GPIO18 |
| RESETN | 17 | IO | I/Pull-up | - |

PIO State After Power-On

| Name | Pin | When RESET_N is low | When RESET_N is high, it enters Boot ROM mode, and waits for a firmware update request. | | | When RESET_N is high, if no firmware update request is detected, it proceeds to firmware execution. |
| --- | --- | --- | --- | --- | --- | --- |
| | | | D_SEL==1 | D_SEL==0 BOOT_MODE==1 | D_SEL==0 BOOT_MODE==0 | |
| PIO0 | 25 | GPIO, input with weak pull-up | GPIO, input with weak pull-up | GPIO, input with weak pull-up | GPIO, input with weak pull-up | Depending on the firmware |
| PIO1 | 28 | GPIO, input with weak pull-up | GPIO, input with weak pull-up | GPIO, input with weak pull-up | GPIO, input with weak pull-up | Depending on the firmware |

| Name | Pin | When RESET_N is low | When RESET_N is high, it enters Boot ROM mode, and waits for a firmware update request. | | | When RESET_N is high, if no firmware update request is detected, it proceeds to firmware execution. |
|---|---|---|---|---|---|---|
| | | | D_SEL==1 | D_SEL==0 BOOT_MODE==1 | D_SEL==0 BOOT_MODE==0 | |
| PIO2 | 27 | GPIO, input with weak pull-up | GPIO, input with weak pull-up | GPIO, input with weak pull-up | GPIO, input with weak pull-up | Depending on the firmware |
| PIO3 | 30 | GPIO, input with weak pull-up | GPIO, input with weak pull-up | GPIO, input with weak pull-up | GPIO, input with weak pull-up | Depending on the firmware |
| PIO4 | 26 | GPIO, input with weak pull-up | GPIO, input with weak pull-up | GPIO, input with weak pull-up | GPIO, input with weak pull-up | Depending on the firmware |
| PIO5 | 29 | GPIO, input with weak pull-up | GPIO, input with weak pull-up | GPIO, input with weak pull-up | GPIO, input with weak pull-up | Depending on the firmware |
| TX | 19 | GPIO, input with weak pull-up | TX, output | GPIO, input with weak pull-up | SPIS_MISO, input with weak pull-up or output | Depending on the firmware |

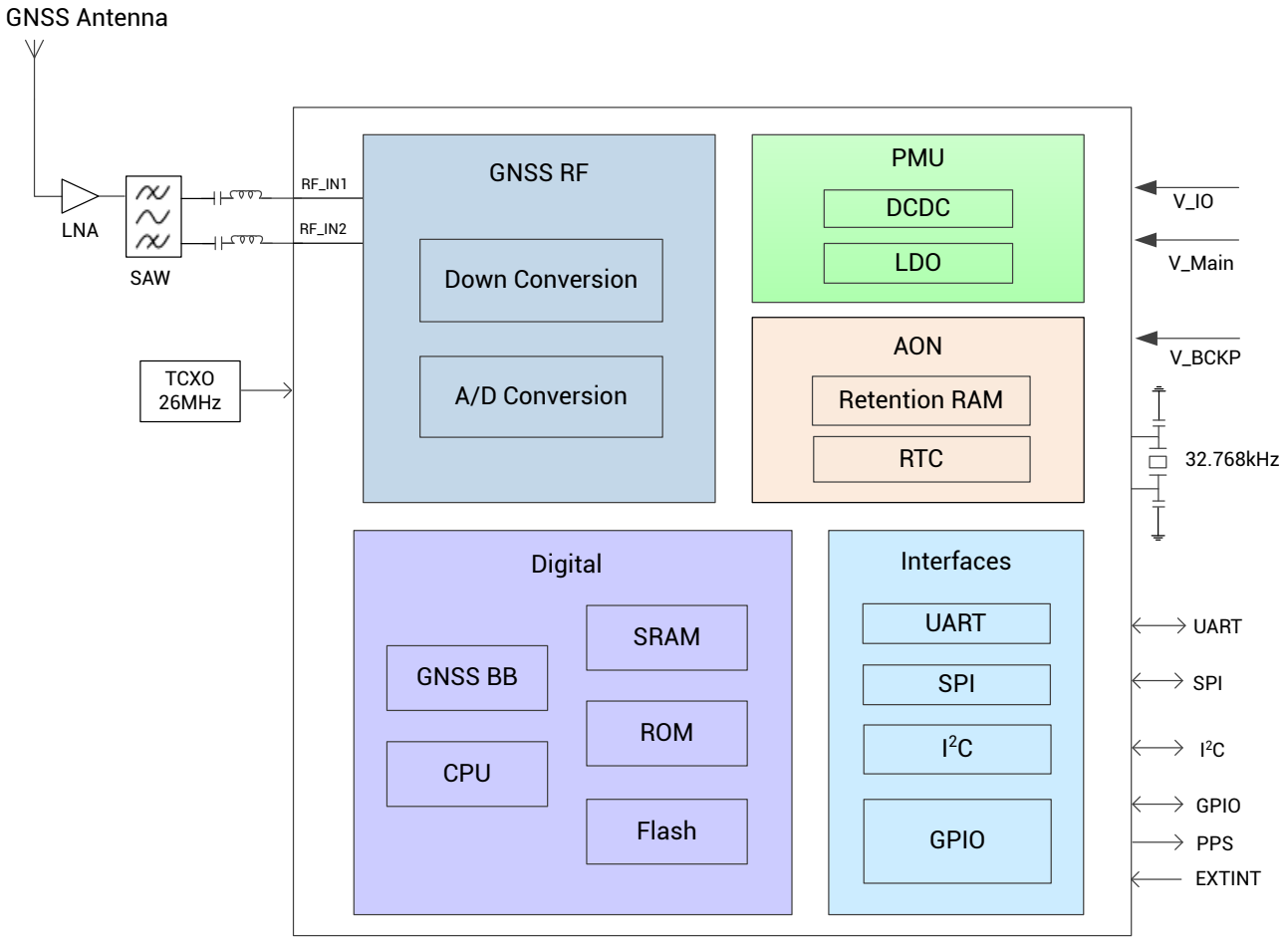
| Name | Pin | When RESET_N is low | When RESET_N is high, it enters Boot ROM mode, and waits for a firmware update request. | | | When RESET_N is high, if no firmware update request is detected, it proceeds to firmware execution. |
|---|---|---|---|---|---|---|
| | | | D_SEL==1 | D_SEL==0 BOOT_MODE==1 | D_SEL==0 BOOT_MODE==0 | |
| RX | 18 | GPIO, input with weak pull-up | RX, input with weak pull-up | GPIO, input with weak pull-up | SPIS_MOSI, input with weak pull-up | Depending on the firmware |
| SCL | 31 | GPIO, input with weak pull-up | SCL, input with weak pull-up | GPIO, input with weak pull-up | SPIS_CLK, input with weak pull-up | Depending on the firmware |
| SDA | 32 | GPIO, input with weak pull-up | SDA, input with weak pull-up | GPIO, input with weak pull-up | SPIS_CSN, input with weak pull-up | Depending on the firmware |
| D_SEL | 33 | GPIO, input with weak pull-up | GPIO, input with weak pull-up | GPIO, input with weak pull-up | GPIO, input with weak pull-up | Depending on the firmware |
| PPS | 35 | GPIO, input with weak pull-up | GPIO, input with weak pull-up | RX, input with weak pull-up | GPIO, input with weak pull-up | Depending on the firmware |

| Name | Pin | When RESET_N is low | When RESET_N is high, it enters Boot ROM mode, and waits for a firmware update request. | | | When RESET_N is high, if no firmware update request is detected, it proceeds to firmware execution. |
|---|---|---|---|---|---|---|
| | | | D_SEL==1 | D_SEL==0 BOOT_MODE==1 | D_SEL==0 BOOT_MODE==0 | |
| BOOT_MODE | 34 | GPIO, input with weak pull-up | GPIO, input with weak pull-up | TX, output | GPIO, input with weak pull-up | Depending on the firmware |
| PIO13 | 14 | GPIO, input with weak pull-up | GPIO, input with weak pull-up | GPIO, input with weak pull-up | GPIO, input with weak pull-up | Depending on the firmware |
| PIO14 | 13 | GPIO, input with weak pull-up | GPIO, input with weak pull-up | GPIO, input with weak pull-up | Event mask output 0 | Depending on the firmware |
| PIO15 | 36 | GPIO, input with weak pull-up | GPIO, input with weak pull-up | GPIO, input with weak pull-up | GPIO, input with weak pull-up | Depending on the firmware |
| PIO16 | 37 | GPIO, input with weak pull-up | GPIO, input with weak pull-up | GPIO, input with weak pull-up | GPIO, input with weak pull-up | Depending on the firmware |

| Name | Pin | When RESET_N is low | When RESET_N is high, it enters Boot ROM mode, and waits for a firmware update request. | | | When RESET_N is high, if no firmware update request is detected, it proceeds to firmware execution. |
|---|---|---|---|---|---|---|
| | | | D_SEL==1 | D_SEL==0 BOOT_MODE==1 | D_SEL==0 BOOT_MODE==0 | |
| PIO17 | 16 | GPIO, input with weak pull-up | GPIO, input with weak pull-up | GPIO, input with weak pull-up | GPIO, input with weak pull-up | Depending on the firmware |
| PIO18 | 15 | GPIO, input with weak pull-up | GPIO, input with weak pull-up | GPIO, input with weak pull-up | GPIO, input with weak pull-up | Depending on the firmware |

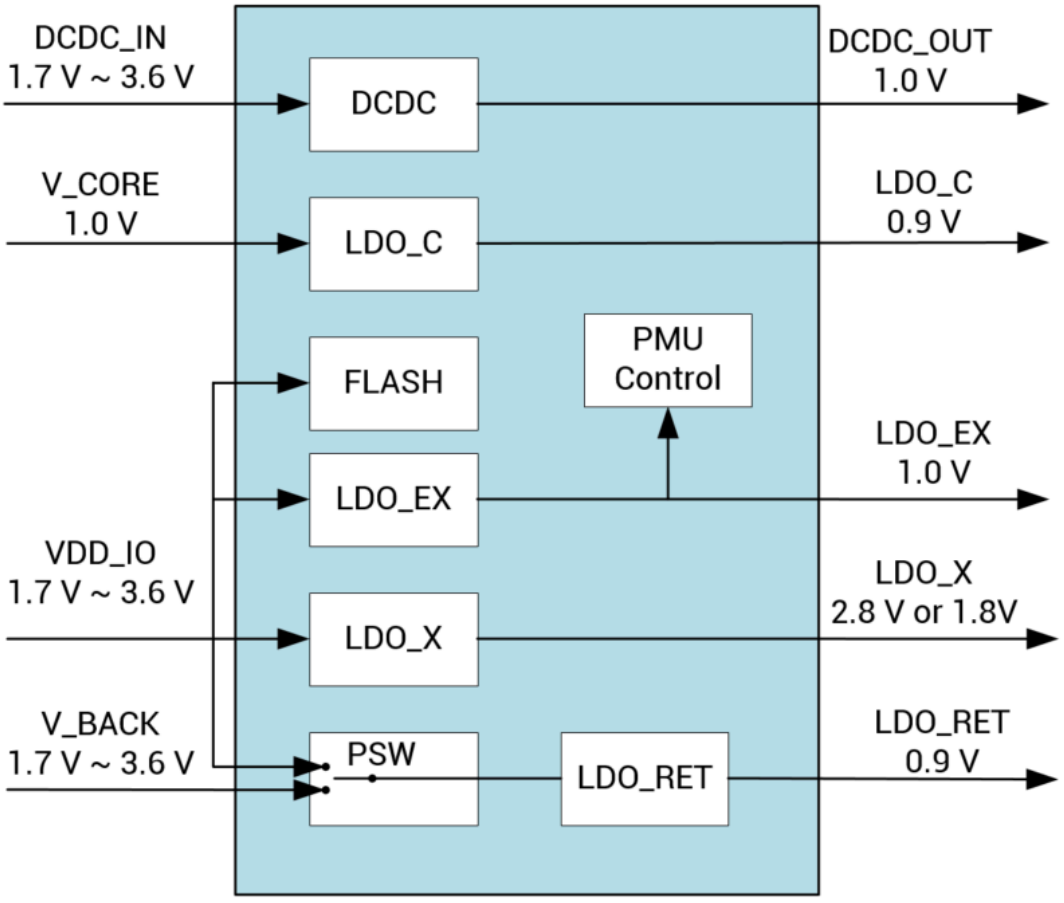
# Chip Structure

## 3.1 Block Diagram



# 3.2 Power Management Unit

The Power Management Unit (PMU) provides four power domains that are internally generated by LDOs and supervised by several voltage monitors:




### Core

Core domain is the main power domain for the RF and digital part inside the chip. It is powered by V_CORE, which is connected to LDO_EX or DCDC_OUT. The subsequent LDO_C converts the V_CORE input to respective voltages, which must be connected with a decoupling capacitor through the LDO_C pin. LDO_C drives the digital logic parts.

### IO

IO power domain is powered by VDD_IO, including the chip IO devices, on-chip Flash, etc. The voltage supply of VDD_IO is 1.7 V to 3.6 V. Except IO devices, other PMU devices are powered by a dedicated LDO_EX. LDO_EX must be connected with a decoupling capacitor through LDO_EX pin.

### Backup

Backup domain runs the RTC section and Retention RAM. This domain uses VDD_IO and V_BACK as the voltage sources. When the range of VDD_IO is normal, it uses VDD_IO, otherwise uses V_BACK. The allowed range of V_BACK is 1.7 V to 3.6 V. If you do not need the RTC and backup function, you must connect the V_BACK pin to VDD_IO.

TCXO

The clock domain supplies power to TCXO. This domain has a dedicated LDO called LDO_X, which is also powered by VDD_IO. If TCXO is powered by LDO_X, LDO_X should be connected to the power pin of TCXO and be decoupled by a capacitor. You can also choose an external power source other than LDO_X to power TCXO.

Based on the above division of power domains and hardware design, UC6580x-00 has three modes of power consumption:

- Running mode: Every power source of the chip is normal, CPU runs normally, and the power supply of each domain is set by the software. All events, including external interruption, communication request, timing, etc., can be processed normally.
- V_BACK mode: The IO and main power supply of the chip is cut off from the outside, and there is only V_BACK power supply left. At this time, the power consumption of the chip drops to a very low level, and the specific functions and power consumption depend on the mode set by the software. It can wake up as soon as it is powered on.
- Power off mode: All power supplies are cut off from the outside, and the chip does not work at all.

## 3.3 Clock

The chip requires an external 26 MHz clock, which is generated by TCXO, to provide reference frequency for RF and baseband PLL. In order to ensure the stable operation of the PLL when the chip is booted, the 26 MHz clock should work stably within 10 ms after the main and IO domains are powered.

The chip supports RTC crystal input. RTC crystal is usually driven by an on-chip 32.768 kHz oscillator, which connects to an external 32.768 kHz crystal. The chip also supports external RTC clock input. The input signal amplitude is required to be from 0.9 V to 1.98 V, and the input signal frequency is required to be 32.768 kHz. The RTC clock frequency offset must be less than 20 ppm.

> **Note**
>
> When using an external RTC clock input to the RTC_I pin, the power-on sequence of the external RTC clock must not be later than that of the V_BACK and VDD_IO of the UC6580x-00. This prevents potential damage to the external RTC clock chip, which could occur if the RTC_I pin outputs a voltage while the external clock chip is not powered on.

| | Frequency Source | Frequency | Remark |
|---|---|---|---|
| **System Clock** | TCXO | 26 MHz | Work stably within10 ms after the main and IO domains are powered |
| **RTC Clock** | On-chip oscillator | 32.768 kHz | Connect an external 32.768 kHz crystal |
| | External digital waveform generator | 32.768 kHz | Input signal amplitude should be 0.9 V to 1.98 V |

If the main power supply and IO power supply fail and a backup power is connected to V_BACK, the baseband, RF and CPU do not work, while RTC keeps running to provide time reference for the receiver. This operating mode is called RTC time keeping mode. Under this mode, the relevant data are saved in Flash for GNSS hot start.

RTC time keeping mode is a prerequisite for GNSS hot start. Under this mode, RTC provides time information; Flash provides ephemeris and almanac information. If you do not need GNSS hot start function, connect RTC_O to ground. In the AGNSS-based system, if time and ephemeris are provided through network as assistance, RTC is not necessary.

| Mode | Power Supply | Working Parts | | | | |
|---|---|---|---|---|---|---|
| | | BB | RF | CPU | RTC | Flash |
| RTC Time Keeping | V_BACK | | | | √ | √ |

## 3.4 System Reset

According to the power structure of UC6580x-00, there are two reset domains: Core domain and Backup domain.

Core domain can be reset by three methods:

- RESETN is the reset pin of the chip. When the voltage level at RESETN is low, the reset signal will be sent to the Core domain. The duration of RESETN low level should be more than 5 ms.
- The chip's software reset, which is controlled by the firmware.
- Watchdog RESET.

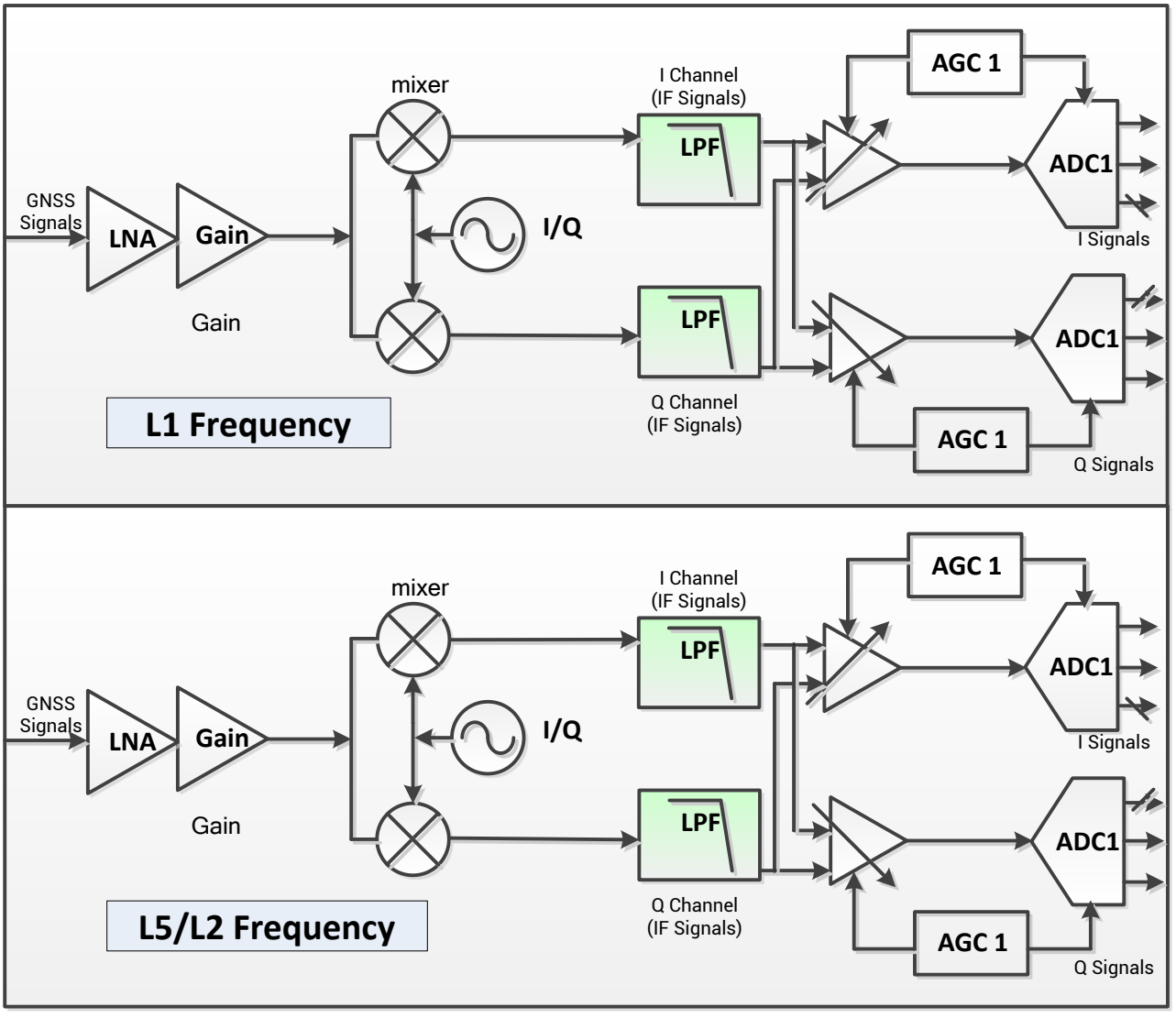
If any of the above reset sources issues a reset signal, the Core domain is reset.

Backup domain can be reset by two methods:

- When the voltage of V_BACK is lower than 1.2 V, it will trigger the reset.
- The software system sends the RTC RESET signal, which is controlled by the firmware and only resets the RTC counter.

# RF Subsystem

The RF subsystem of UC6580x-00 adopts dual-frequency dual-channel architecture. The frequency of the input signal ranges from 1166 MHz to 1620 MHz. The received GNSS signals are amplified by a single-ended Low Noise Amplifier (LNA), and then fed to a RF gain block to be further amplified, thus reducing the noise figure requirements for the mixer. The RF gain block also provides a single-ended to differential conversion. After completing the orthogonal down-conversion, multi-GNSS signals are divided into two channels. Afterwards, the I and Q signals of both channels are low-pass filtered and amplified by a separate Programmable Gain Amplifier (PGA), after which both I and Q signals are sent to the high-speed ADC section for data conversion.




The RF subsystem of UC6580x-00 supports any mode below:

- Dual-frequency L1+L5
- Dual-frequency L1+L2

- L1 single-frequency multi-constellation mode.

## 4.1 LNA

The low noise amplifier (LNA) makes use of a single stage configuration and requires external matching to function satisfactorily. For improved performance, an external LNA should be added, of which the gain range is recommended to be within 17dB to 50dB. In an environment with complex interference, it is necessary to use an external SAW filter to suppress out-of-band interference.

## 4.2 Gain Block

A single stage differential amplifier follows the LNA providing further amplification and conversion from single-ended signals to differential signals.

## 4.3 Mixer

UC6580x-00 uses the active I/Q mixer to first convert the multi-GNSS signals to an intermediate frequency signals. At this stage, the signals are split into two IF channels after down-conversion.

## 4.4 IF Filter

UC6580x-00 integrates an I/Q low-pass filter to remove the out-of-band noise after RF down-conversion, which improves the noise performance of the RF system.

## 4.5 AGC

UC6580x-00 supports Automatic Gain Control (AGC), which reduces the convergence time and computing cost. AGC controls the gain configuration of each module in the radio frequency data link according to the signal energy required by the RF system.

## 4.6 PGA and ADC

UC6580x-00 integrates Programmable Gain Amplifier (PGA) and high-speed Analog Digital Convertor (ADC). The gain value of PGA is configured by AGC to ensure that the signal energy output by ADC remains unchanged when the RF input signal energy changes within a certain range, thereby ensuring that the output of the high-speed ADC does not saturate. The high-speed ADC supports the output of I/Q complex sampling signals.

# Baseband Subsystem

UC6580x-00 provides multiple interfaces for data communication or access to external devices, such as UART, SPI, I2C, GPIO, etc.

This chapter covers the following aspects:

- Interfaces
- PIO Functions
- Time Management Unit
- Watchdog
- Timer Counter

## 5.1 Interfaces

### 5.1.1 UART

UC6580x-00 makes use of two UART interfaces: UART1 and UART2. Both of them can be used for communication with a host.

By default, PIO6/PIO7 corresponds to UART1, which serves as the main UART in standard firmware version. The communication interface of UC6580x-00 can be mapped to different PIO interfaces via BOOT_MODE. PIO6/PIO7 can also be used as SPI, and in this case, there is no UART1 function. See the description in section Firmware Upgrade Mode for the use of BOOT_MODE and the corresponding communication interface mapping.

UART2 can use PIO15/PIO16. It is mainly used for transmitting or debugging auxiliary information.

### 5.1.2 SPI slave

UC6580x-00 uses SPI slave interface as an optional way to communicate with the host to transfer data. At the same time, it supports loading firmware via the SPI slave interface. The maximum transmission rate using SPI slave is 8 Mbps, and the maximum SPI clock frequency is 8 MHz. When the SPI slave loads the firmware, the maximum transmission rate is 4 Mbps.

The SPI slave interface shares PIO6/PIO7 and PIO8/PIO9 with UART1 and I2C respectively. Users can select the communication interface via D_SEL and BOOT_MODE. If PIO6/PIO7/PIO8/PIO9 is used as SPI slave interface, there are no UART1 and I2C1 functions; if PIO6/PIO7 and PIO8/PIO9 are used as UART1 and I2C1, there is no SPI slave interface.

When the SPI slave interface is used for host communication, PIO14 should be used as the SRDY (Slave Ready) signal to indicate whether the SPI slave is ready.

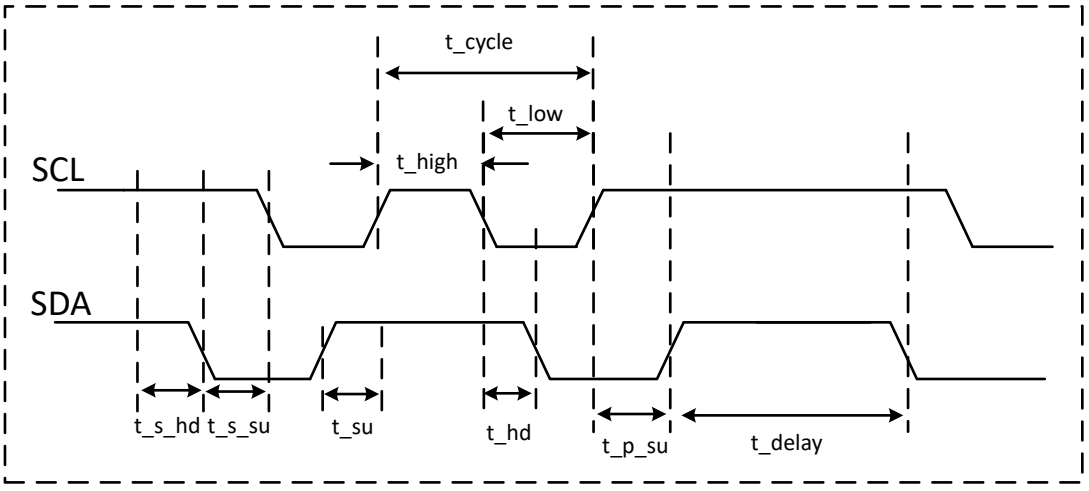
## 5.1.3 SPI master

UC6580x-00 provides SPI master interface by configuring PIO0/PIO1/PIO4/PIO5, which can be used to communicate with or control other SPI slave devices. The maximum transmission rate of the SPI master interface is 16 Mbps, and the maximum SPI clock frequency is 16 MHz.

The SPI master interface is disabled by default.

## 5.1.4 I2C

UC6580x-00 provides one I2C interface (I2C1) to load firmware and communicate with the host. The I2C1 works in slave mode. It is compatible with the I2C protocol, supporting the transmission rates of 100 Kbps, 400 Kbps and 3.4 Mbps. The current firmware supports 400 Kbps transmission. By default, the I2C1 uses PIO8/PIO9, and the BOOT_MODE pin should be in pull-up or open-circuit state when booting. For more information, please see the description in section PIO Functions.




I2C Timing Requirement

| Symbol | Parameter | Min. | Max. | unit |
|---|---|---|---|---|
| t_cycle | SCL clock period | 100 | 3400 | kbps |
| t_high | High period of SCL clock | 0.06 | 5 | μs |
| t_low | Low period of SCL clock | 0.16 | 5 | μs |
| t_su | Data setup time | 0.072 | | μs |
| t_hd | Data hold time | 0.072 | | μs |
| t_s_su | Setup time for start condition | 0.072 | | μs |

| Symbol | Parameter | Min. | Max. | unit |
|---|---|---|---|---|
| t_s_hd | Hold time for start condition | 0.072 | | μs |
| t_p_su | Setup time for stop condition | 0.072 | | μs |
| t_delay | Delay time between a start and stop condition | 0.5 | | μs |

### 5.1.5 Serial Flash Interface

Serial Flash interface is used to connect UC6580x-00 with external SPI Flash. SPI Flash can be used for firmware storage and update.

The serial Flash interface uses PIO0/PIO1/PIO2/PIO3/PIO4/PIO5 only when the BOOT_MODE pin is in pull-up or open-circuit state when booting; otherwise, the serial Flash interface is invalid.

## 5.2 PIO Functions

The PIO module may be configured as GPIO or as the aforementioned communication interfaces. The following table describes all PIO functions.

| PIO # | Default Function | I/O | Description | Alternate Function |
|---|---|---|---|---|
| 0 | GPIO | I/O | - | SPI master MISO<br>SPI flash D0 |
| 1 | GPIO | I/O | - | SPI master MOSI<br>SPI flash D1 |
| 2 | GPIO | I/O | - | PWM0<br>UART2 RXD<br>SPI flash WP |
| 3 | GPIO | I/O | - | PWM1<br>UART2 TXD<br>SPI flash HOLD |
| 4 | GPIO | I/O | - | SPI master CLK<br>SPI flash CLK |
| 5 | GPIO | I/O | - | SPI master CSN<br>SPI flash CSN |

| PIO # | Default Function | I/O | Description | Alternate Function |
|---|---|---|---|---|
| 6 | GPIO | I/O | Controlled by BOOT_MODE when booting:<br>UART1 TXD (if BOOT_MODE is high when booting)<br>SPI slave MISO (if BOOT_MODE is low when booting) | UART1 TXD<br>SPI slave MISO |
| 7 | GPIO | I/O | Controlled by BOOT_MODE when booting:<br>UART1_RXD (if BOOT_MODE is high when booting)<br>SPI slave MOSI (if BOOT_MODE is low when booting) | UART1 RXD<br>SPI slave MOSI |
| 8 | GPIO | I/O | Controlled by BOOT_MODE when booting:<br>I2C1 SCL (if BOOT_MODE is high when booting)<br>SPI slave CLK (if BOOT_MODE is low when booting) | I2C1 SCL<br>SPI slave CLK |
| 9 | GPIO | I/O | Controlled by BOOT_MODE when booting:<br>I2C1 SDA (if BOOT_MODE is high when booting)<br>SPI slave CSN (if BOOT_MODE is low when booting) | I2C1 SDA<br>SPI slave CSN |
| 10 | GPIO | I/O | Communication interface selection pin.<br>Select from PIO6 to PIO9.<br>Only valid when booting.<br>This pin is pulled up if it is not connected. | PPS<br>D_SEL<br>32.768 kHz clock out |
| 11 | GPIO | I/O | - | PPS<br>EVENT<br>UART1 RXD |

| PIO # | Default Function | I/O | Description | Alternate Function |
|---|---|---|---|---|
| 12 | GPIO | I/O | Bootstrap mode selection pin.<br>Select firmware loading address, external/internal Flash or SPI interface.<br>Only valid when booting.<br>This pin is pulled up if it is not connected. | BOOT MODE<br>PPS<br>RF_READY<br>UART1 TXD |
| 13 | GPIO | I/O | - | ODO_DIR<br>EVENT |
| 14 | GPIO | I/O | - | ODO_CNT<br>EVENT |
| 15 | GPIO | I/O | - | UART2 TXD<br>LO1_DET |
| 16 | GPIO | I/O | - | UART2 RXD<br>BLK<br>LO2_DET |
| 17 | GPIO | I/O | - | ODO_DR |
| 18 | GPIO | I/O | - | ODO_CNT |

> If you want to change the I/O alternate function, please contact the Unicore FAE.

## 5.3 Time Management Unit

The Time Management Unit (TMU) manages all clock sources in the baseband, using more accurate clocks to calibrate less accurate clocks.

## 5.4 Watchdog

UC6580x-00 contains two watchdog timers which prevent the system-lockup caused by the software deadlock. During normal operation, the firmware resets the watchdog's internal counter at regular intervals before the timer overflow occurs.

## 5.5 Timer Counter

The timer counter has an EVENT input and a PPS output.

EVENT can be input via PIO11, PIO13 or PIO14, but only one EVENT can be input at a time. Event input is the external timestamp event relative to GPS time.

> EVENT function is disabled by default. Please contact Unicore FAE if necessary.

PPS can be output via PIO11. PPS outputs pulse sequence synchronized with GPS or UTC time grid, and the time interval can be configured over a wide range of frequency.

All input and output signals are synchronized with the internal clock frequency of the receiver, so that the inherent maximum quantization error of the input and output signals reaches ±10 ns.

# System Configuration

## 6.1 Power Supply Scheme

UC6580x-00 supports two power supply schemes, including internal DC-DC mode and LDO mode.

> DCDC_IN and VDD_IO use the same power.
>
> V_BACK can use an independent power, or use the same power as DCDC_IN and VDD_IO.
>
> TCXO is powered by LDO_X. The voltage could be 1.8 V or 2.8 V[1].
>
> To prevent reverse current flowing from VDD_IO to V_BACK, the supply voltage of V_BACK should be no lower than VDD_IO or you should add a forward biased diode before V_BACK. Meanwhile, make sure that V_BACK is within the range of 1.7 V to 3.6 V. The diode is recommended to be of low power (mA-level forward current), low forward voltage drop (300 mV), and low reverse leakage current (< 100 μA within the working temperature).
>
> If you do not use the hot start and backup function, connect the V_BACK to VDD_IO

### 6.1.1 DC-DC Mode

In this mode, the main power (V_Main) connects to the pin DCDC_IN, and the output of the DCDC module DCDC_OUT provides the power to the rest circuits. At this time, the system is powered by the internal DC-DC:

- The system power supply is input to the DCDC_IN, and output from the DCDC_OUT, which is connected to the V_CORE input pin via a power inductor.

### 6.1.2 LDO Mode

In this mode, the main power (V_Main) connects to DCDC_IN while DCDC_IN and DCDC_OUT are short-circuited and the internal DC-DC is bypassed, so that the V_Main provides the power to the rest circuits directly. At this time:

- DCDC_IN and DCDC_OUT are short-circuited together.
- The system power supply is input by VDD_IO and output to V_CORE through LDO_EX.

For specific design scheme of the above modes, please refer to *UC6580x-00 Hardware Reference Design*.

[1]. The output voltage of LDO_X is determined at the manufacturing of the chip and cannot be changed by firmware. The current mass-produced chips have an output of 1.8V. If you need a 2.8V output, please contact Unicore in advance.

## 6.2 Firmware Upgrade Mode

The UC6580x-00 chip supports three firmware upgrade modes, which is controlled by the D_SEL pin (PIO 10) and BOOT_MODE pin (PIO 12).

- Mode 1: firmware upgrade through UART1 (PIO6 and PIO7) or I2C1 (PIO8 and PIO9).
- Mode 2: firmware upgrade through UART1 (PIO11 and PIO12).
- Mode 3: firmware upgrade through SPI slave (PIO6 to PIO9).

See the following tables for the configuration of the pins at boot when upgrading the firmware.

BOOT_MODE is valid only at power-on or before the RESETN signal is sent. After the RESETN signal is sent, the BOOT_MODE pin can be used as an ordinary PIO pin.

**Pin Configurations at Boot**

| Mode | D_SEL | BOOT_MODE | Boot Mode | At Boot | | | Remark |
|---|---|---|---|---|---|---|---|
| | | | | PIO 6/7 | PIO 8/9 | PIO 11/12 | |
| Mode 1 | 1 | X | Boots from UART1 and I2C1 | UART1 | I2C1 | X | |
| Mode 2 | 0 | 1 | Boots from UART1 | X | X | UART1 | Boots from UART1 (PIO11 and PIO12), no I2C1 boot |
| Mode 3 | 0 | 0 | Boots from SPI slave | SPI slave | SPI slave | X | |

The boot steps are as follows:

Step 1: CPU detects the firmware upgrade request from the interfaces.

- Mode 1

| If | Then |
| --- | --- |
| CPU detected a firmware upgrade request from UART1 within 40 ms after power-on or reset. | CPU starts to adapt the baud rate and upgrade the firmware. After the upgrade, run the firmware. |
| CPU detected a firmware upgrade request from I2C1 within 40 ms after power-on or reset. | CPU starts to adapt the I2C1 clock and upgrade the firmware. After the upgrade, run the firmware. |
| CPU detected a firmware upgrade request from both UART1 and I2C1 within 40 ms after power-on or reset. | Initialize the interface whose baud rate has been identified first, and read the upgrade request from that interface. After the upgrade, run the firmware. |
| CPU has not detected any firmware upgrade request from UART1 or I2C1 within 40 ms after power-on or reset. | Do step 2 |

- Mode 2

| If | Then |
| --- | --- |
| CPU detected a firmware upgrade request from UART1 within 40 ms after power-on or reset. | CPU starts to adapt the baud rate and upgrade the firmware. After the upgrade, run the firmware. |
| CPU has not detected any firmware upgrade request from UART1 within 40 ms after power-on or reset. | Do step 2 |

- Mode 3

| If | Then |
| --- | --- |
| CPU detected a firmware upgrade request from SPI slave within 40 ms after power-on or reset. | CPU upgrades the firmware and runs it after the upgrade. |
| CPU has not detected any firmware upgrade request from SPI slave within 40 ms after power-on or reset. | Do step 2 |

Step 2: CPU detects the built-in flash and external flash in order.

- CPU Detects Flash

| If | Then |
| --- | --- |
| CPU detected a firmware in the built-in flash. | CPU reads the firmware and runs it. |
| CPU has not detected any firmware in the built-in flash. | CPU tries to read the firmware in the external flash and runs it. |

# Electrical Specifications

This chapter covers the electrical specifications of the UC6580 series chips.

The operating temperature range for UC6580A-00 is -40°C to 105°C, and for UC6580I-00 it is -40°C to 85°C.

These temperature conditions apply to all electrical specifications described in this chapter.

## 7.1 DC Electrical Specifications

### 7.1.1 Absolute Maximum Ratings

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| DCDC_IN | Input voltage of the internal DC/DC converter | -0.2 | 3.6 | V |
| DCDC_OUT | Output voltage of the internal DC/DC converter, externally connected to an inductor and two filter capacitors to provide 1.0 V power. The recommended inductance is 1 μH and the recommended capacitance is 10 μF. | -0.2 | 1.05 | V |
| VDD_IO | Input voltage of I/O, LDO_X and flash | -0.2 | 3.6 | V |
| V_BACK | Supply voltage of backup domain | -0.2 | 3.6 | V |
| TCXO_IN | Input voltage on TCXO_IN | -0.6 | 2.9 | V |
| RTC_I | Input voltage on RTC_I | -0.2 | 1.98 | V |
| Vidig | Input voltage on PIO | -0.2 | 3.6 | V |
| Prfin | RF input power on LNA_IN | | +15 | dBm |
| Ptot | Total power | | 360 (@room temperature) | mW |
| Tjun | Junction temperature | -40 | +125 | °C |
| Ts | Storage temperature | -50 | +150 | °C |

> The ripple voltage of all the input voltages must be within 50 mV.

### 7.1.2 Recommended Working Conditions

| Symbol | Parameter | Min. | Typical | Max. | Unit |
|---|---|---|---|---|---|
| DCDC_IN | Input voltage of internal DC/DC converter | 1.7 | 3.3 | 3.6 | V |
| VDD_IO | Input voltage of I/O, LDO_X and flash | 1.7 | 3.3 | 3.6 | V |
| V_BACK | Supply voltage of backup domain | 1.7 | 3.3 | 3.6 | V |

## 7.2 Transient Maximum Ratings

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| DCDC_IN | Input voltage of the internal DC/DC converter | -0.6 | 5.0 | V |
| DCDC_OUT | Output voltage of the internal DC/DC converter | -0.6 | 5.0 | V |
| VDD_IO | Input voltage of I/O, LDO_X and flash | -0.6 | 5.0 | V |
| V_BACK | Supply voltage of backup domain | -0.6 | 5.0 | V |
| V_CORE | Supply voltage of baseband main core and RF | -0.6 | 1.5 | V |
| LDO_EX | LDO_EX output voltage, supplying power for CORE and RF | -0.6 | 1.5 | V |
| LDO_C | LDO_C output voltage, supplying power for CORE | -0.6 | 1.5 | V |
| LDO_RET | LDO_RET output voltage, supplying power for AON | -0.6 | 1.5 | V |
| LDO_X | LDO_X output voltage, supplying power for TCXO | -0.6 | 3.3 | V |
| TCXO_IN | Input voltage on TCXO_IN | -0.6 | LDO_X+0.6 | V |
| RTC_I | Input voltage on RTC_I | -0.6 | VDD_IO/V_BACK +0.6 | V |
| Vidig | Input voltage on PIO | -0.6 | VDD_IO+0.6 | V |

## 7.3 PIO Electrical Specifications

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Ileak | Leakage current input pins | | | | 5 | μA |
| Vil | Low level input voltage | | | | 0.2×VDD_IO | V |
| Vih | High level input voltage | | 0.8×VDD_IO | | | V |
| Vol | Low level output voltage | Iout = -5mA | | | 0.4 | V |
| Voh | High level output voltage | Iout = 5mA | VDD_IO-0.55 | | | V |
| Rpu | Pull-up resistance | | 200 | 260 | 320 | kΩ |
| Cap_DIG_IN | Input capacitance of digital IO | | | 0.7 | | pF |

> The PIO output type is push-pull.

## 7.4 Analog Electrical Specifications

**Analog Electrical Specifications 1**

| Symbol | Parameter | Min. | Typical | Max. | Unit |
|---|---|---|---|---|---|
| LDO_X[1] | LDO_X output voltage (1.8 V TCXO) | 1.75 | 1.8 | 1.95 | V |
| | LDO_X output voltage (2.8 V/2.9 V TCXO) | 2.75 | 2.8 | 2.95 | V |
| LDO_RET | LDO_RET output voltage (VDD_IO power on; V_BACK power on) | 0.85 | 0.9 | 0.95 | V |

| Symbol | Parameter | Min. | Typical | Max. | Unit |
|---|---|---|---|---|---|
| | LDO_RET output voltage (VDD_IO power off; V_BACK power on) | 0.55 | 0.65 | 0.75 | V |
| LDO_C | LDO_C output voltage | 0.85 | 0.9 | 0.95 | V |
| LDO_EX | LDO_EX output voltage | 0.95 | 1.0 | 1.05 | V |
| V_DET[2] | Antenna detection input | 2.7 | 3.3 | 3.6 | V |
| VDD_ANT[3] | Antenna power output | 2.7 | 3.3 | 3.6 | V |
| RTC_I | 32.768 kHz crystal or digital waveform input | | | 1.98 | V |
| RTC_O | 32.768 kHz clock output | | | 1.98 | V |
| DCDC_OUT | Output voltage of the internal DC/DC converter, externally connected to an inductor and two filter capacitors to provide 1.0 V power. The recommended inductance is 1 μH and the recommended capacitance is 10 μF. | 0.95 | 1.0 | 1.05 | V |
| TCXO_IN_Vpp | TCXO input peak-to-peak voltage | 0.5 | 0.6 | 1.4 | Vpp |

[1]. The output voltage of LDO_X is determined at the manufacturing of the chip and cannot be changed by firmware. The current mass-produced chips have an output of 1.8V. If you need a 2.8V output, please contact Unicore in advance. ↩

[2]. Not supported currently. ↩

[3].The output voltage of VDD_ANT = V_DET- (antenna current) * (10 Ω). ↩

### Analog Electrical Specifications 2: RTC Specifications

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| RTC_Fxtal | RTC crystal oscillator resonate frequency | | | 32768 | | Hz |

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| RTC_T_start | RTC startup time | | 0.2 | 1 | 2 | s |
| RTC_CL | RTC load capacitance | ESR = 80 kΩ | | 12.5 | | pF |
| RTC_Vil | RTC low level input voltage | Shared RTC oscillator input | 0.0 | | 0.2 | V |
| RTC_Vih | RTC high level input voltage | Shared RTC oscillator input | 0.9 | | 1.98 | V |

## 7.5 RF Electrical Specifications

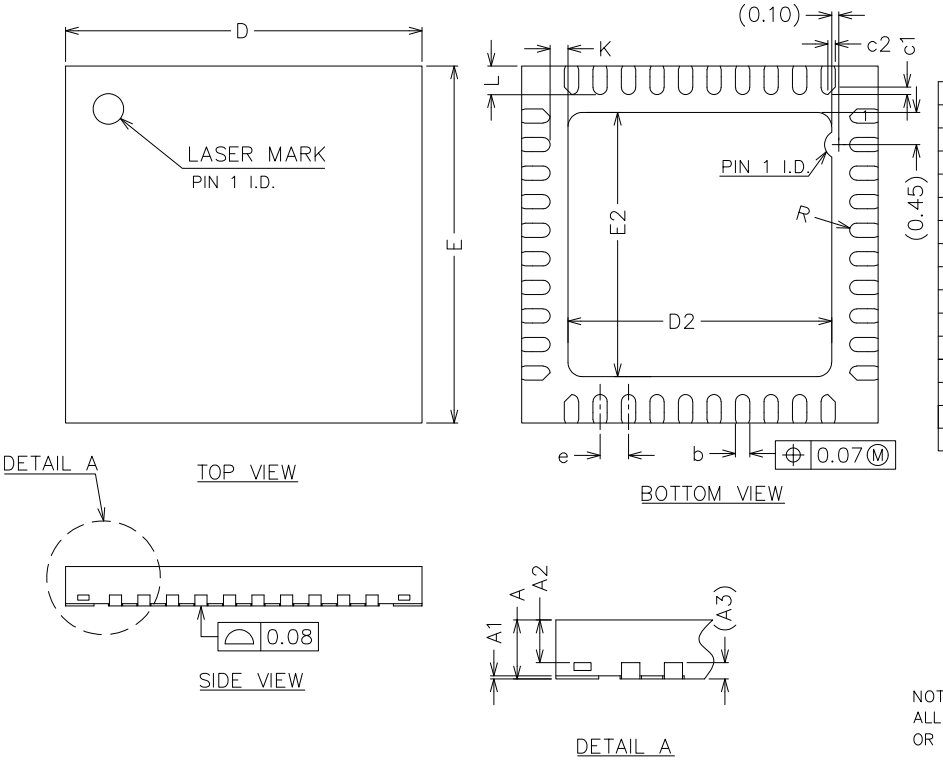
| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| L1_IN | Receiver input frequency | | 1559.098 | 1575.42 | 1606 | MHz |
| L5_IN | Receiver input frequency | | 1166.45 | 1176.45 | 1217.14 | MHz |
| LNA_IN | LNA input impedance | Need matching components and DC blocking capacitors | | 50 | | Ω |
| LNA_S11 | LNA input return loss | 50 Ω environment | | -10 | | dB |
| NFtot | Receiver cascaded noise figure | 50 Ω environment | | 5 | | dB |
| Ext_Gain | External LNA gain | 50 Ω environment | 15 | 17 | 60* | dB |

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| TCXO_Freq | TCXO frequency | 0.5 ppm | | 26 | | MHz |

*. When the external LNA gain falls into this range, the system's CN0 fluctuates by 1dB.↩

# Mechanical Dimensions

## 8.1 UC6580A-00 (QFN40 Automotive)

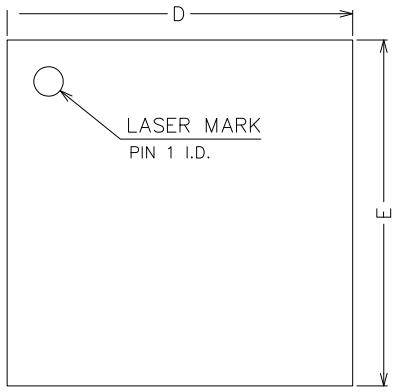


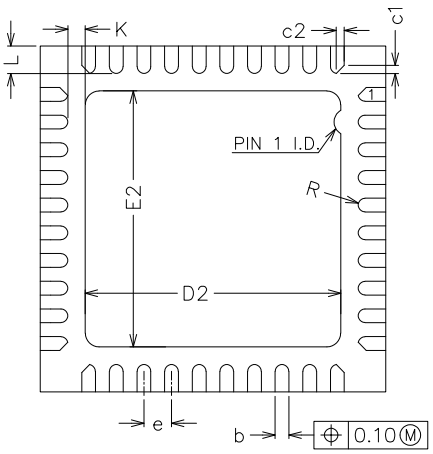

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

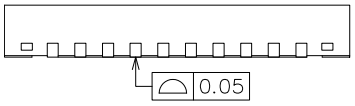
| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| A2 | 0.60 | 0.65 | 0.70 |
| A3 | | 0.20REF | |
| b | 0.15 | 0.20 | 0.25 |
| D | 4.90 | 5.00 | 5.10 |
| E | 4.90 | 5.00 | 5.10 |
| D2 | 3.60 | 3.70 | 3.80 |
| E2 | 3.60 | 3.70 | 3.80 |
| e | 0.35 | 0.40 | 0.45 |
| K | 0.20 | – | – |
| L | 0.35 | 0.40 | 0.45 |
| R | 0.075 | – | – |
| c1 | – | 0.10 | – |
| c2 | – | 0.10 | – |

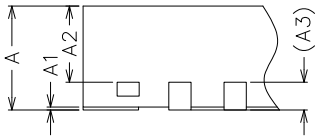
NOTES:
ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION.

# 8.2 UC6580I-00 (QFN40 Industrial)




COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

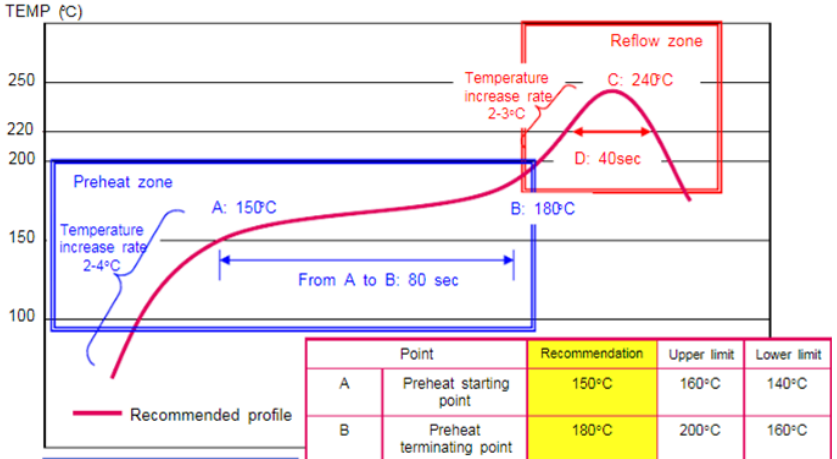
| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0 | 0.02 | 0.05 |
| A2 | 0.60 | 0.65 | 0.70 |
| A3 | | 0.20REF | |
| b | 0.15 | 0.20 | 0.25 |
| D | 4.90 | 5.00 | 5.10 |
| E | 4.90 | 5.00 | 5.10 |
| D2 | 3.60 | 3.70 | 3.80 |
| E2 | 3.60 | 3.70 | 3.80 |
| e | 0.35 | 0.40 | 0.45 |
| K | 0.20 | – | – |
| L | 0.35 | 0.40 | 0.45 |
| R | 0.09 | – | – |
| C1 | – | 0.12 | – |
| C2 | – | 0.12 | – |

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MO-220 WHHE-1.

# Reflow Soldering

## 9.1 Reflow Soldering

The reflow soldering temperature curve is recommended as shown in the figure below (M705-GRN360 is recommended for solder paste).




| Point | | Recommendation | Upper limit | Lower limit |
|---|---|---|---|---|
| A | Preheat starting point | 150°C | 160°C | 140°C |
| B | Preheat terminating point | 180°C | 200°C | 160°C |
| From A to B | Preheating time | 80sec | 100sec | 60sec |
| C | Peak temperature | 240°C | 255°C | 230°C |
| D | Temperature holding time at 220C or higher | 40sec | 60sec | 30sec |

**Reflow oven used for verification**
**SAI-838 (air reflow oven)**
**SNR-825 (nitrogen reflow oven)**

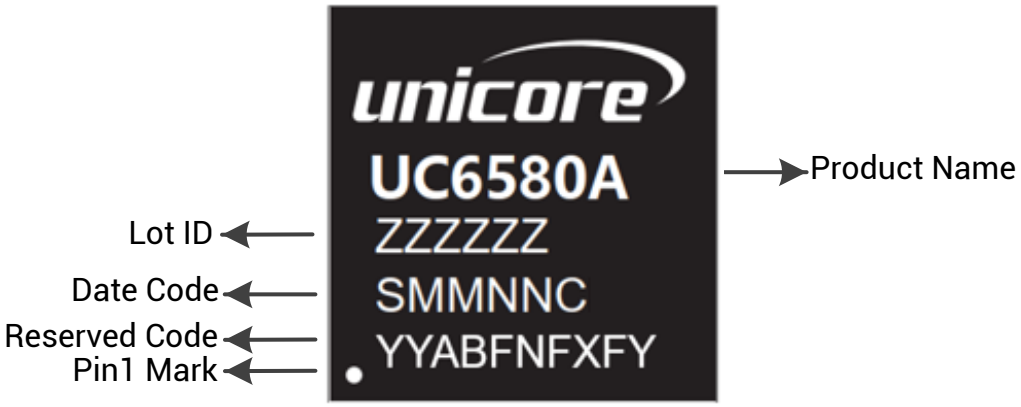
# Product Appearance and Packaging

## 10.1 Product Appearance


UC6580A-00（QFN40 Automotive）


UC6580I-00（QFN40 Industrial）

## 10.2 Label




| Product Model | Description |
| --- | --- |
| UC6580A-00 | Automotive grade |
| UC6580I-00 | Industrial grade |

## 10.3 Moisture Sensitivity Level

The Moisture Sensitivity Levels (MSL) of UC6580A and UC6580I are shown in the table below. Packaging and handling precautions related to the MSL should follow the standard IPC/JEDEC J-STD-033. For more information, visit the JEDEC website.

| Model | MSL |
|---|---|
| UC6580A-00 | MSL 1 |
| UC6580I-00 | MSL 3 |

## 10.4 Ordering Information

| Model | Chip Scale Package | Built-in Flash | Operating Temperature | Grade | Product Package |
|---|---|---|---|---|---|
| UC6580A-00 | QFN40<br>5 mm × 5 mm × 0.85mm | Yes | -40 °C to 105 °C | Automotive | Tape & Reel, 3000 pcs/reel |
| UC6580I-00 | QFN40<br>5 mm × 5 mm × 0.85mm | Yes | -40 °C to 85 °C | Industrial | Tape & Reel, 3000 pcs/reel |

和芯星通科技（北京）有限公司

Unicore Communications, Inc.

北京市海淀区丰贤东路 7 号北斗星通大厦三层
F3, No.7, Fengxian East Road, Haidian, Beijing, P.R.China, 100094
www.unicore.com

Phone: 86-10-69939800

Fax: 86-10-69939888

info@unicorecomm.com